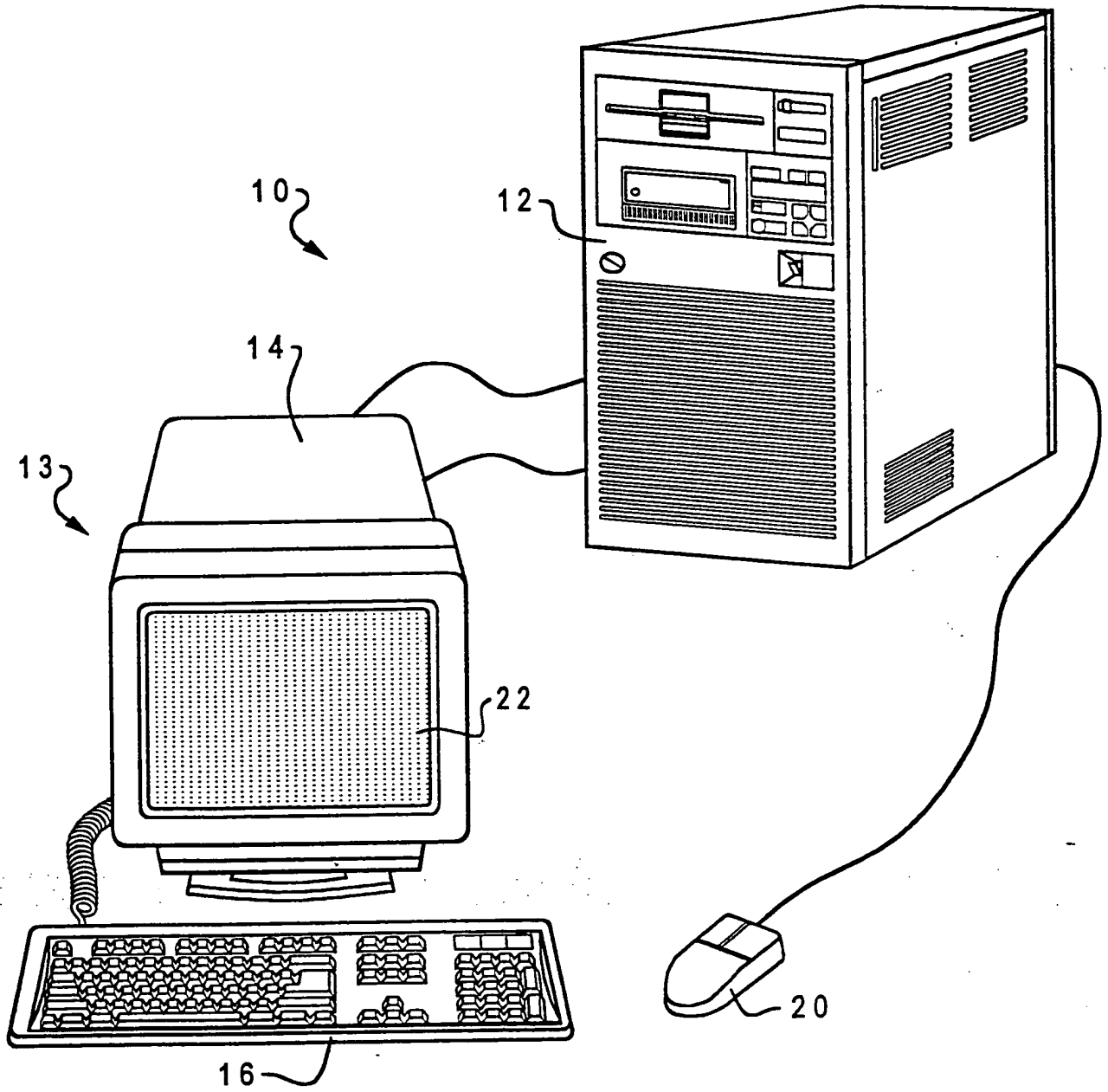

Fig. 1

000627 "T5225760

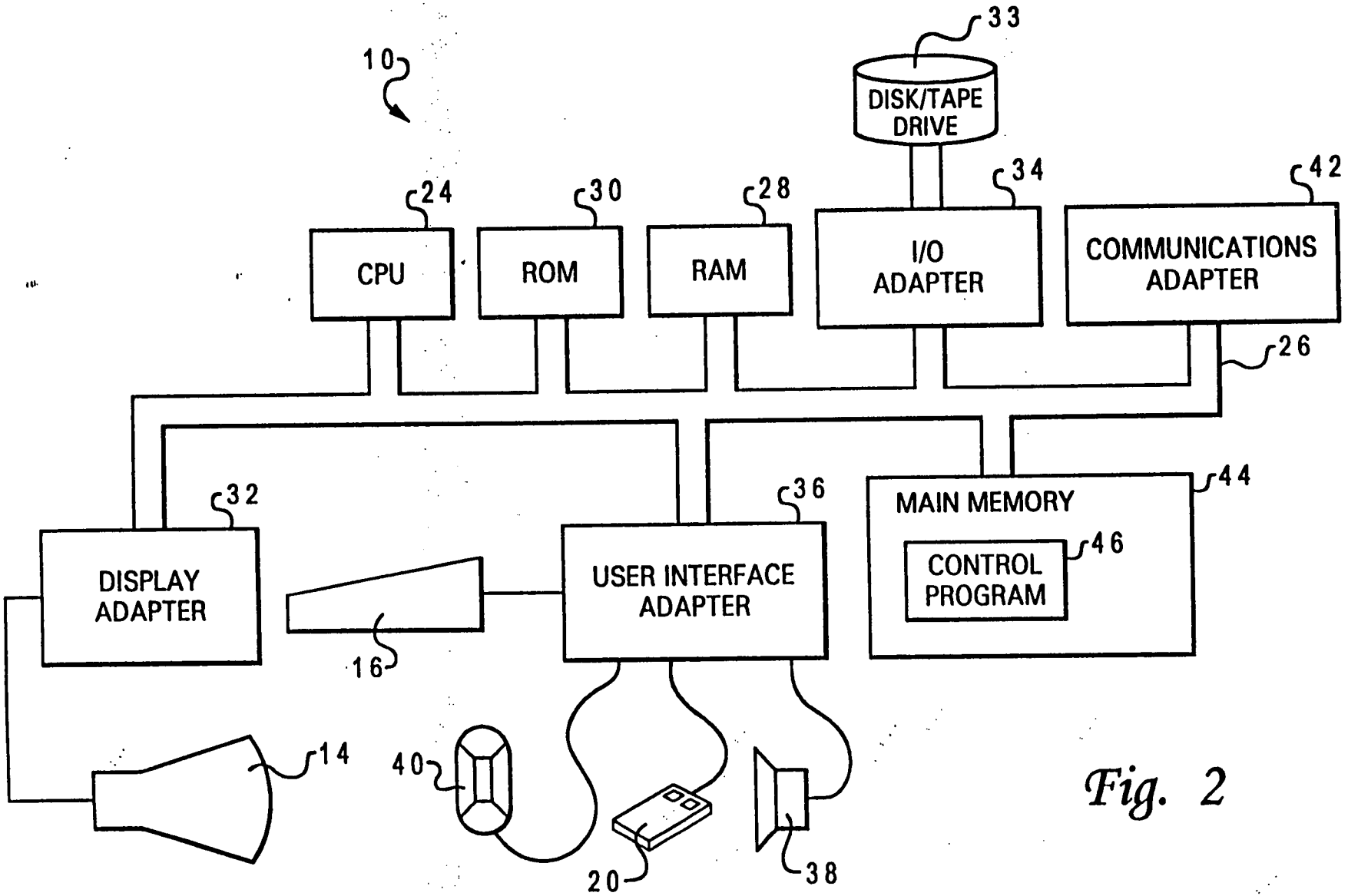

Fig. 2

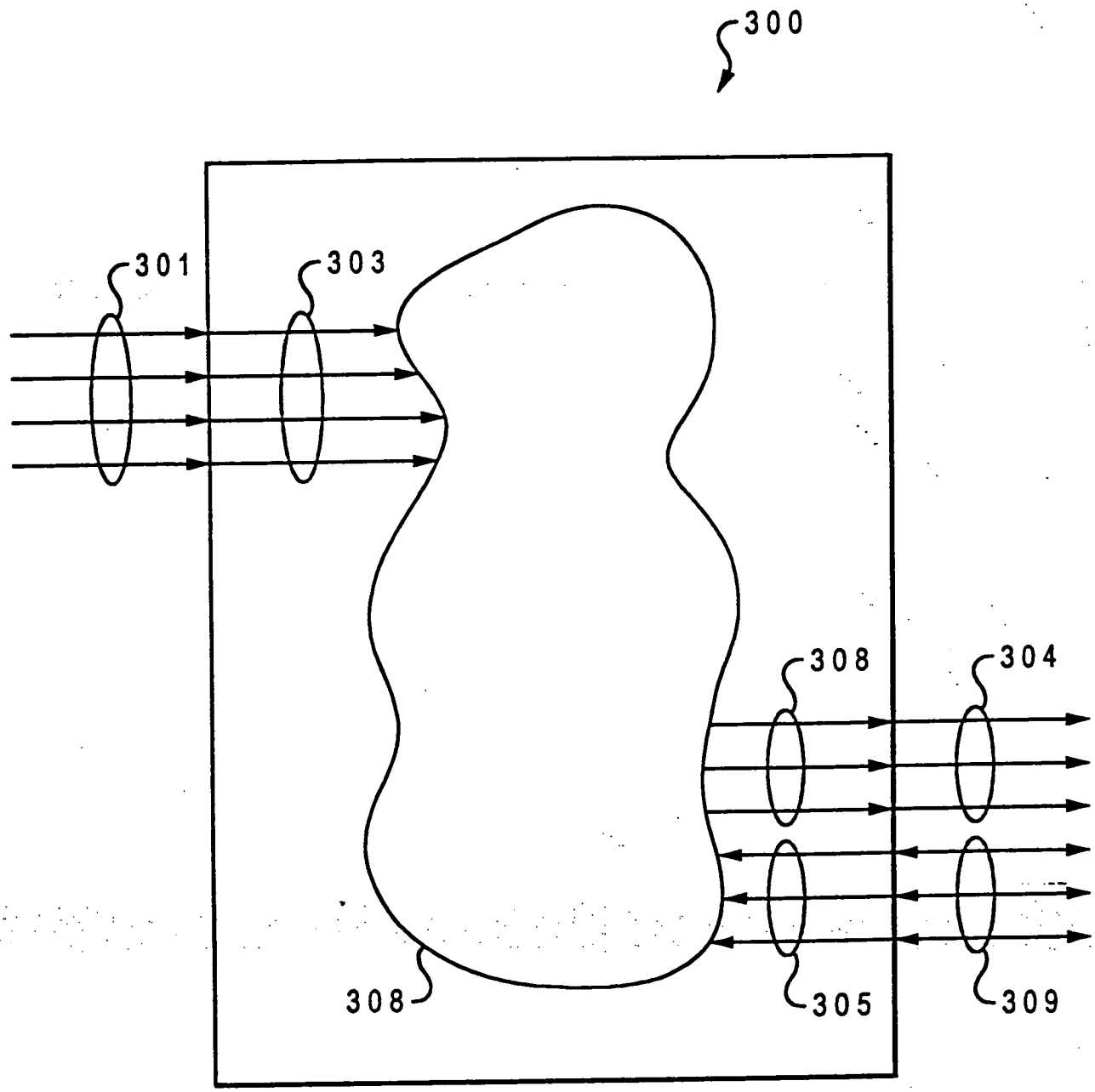

Fig. 3A

00021" T5225760

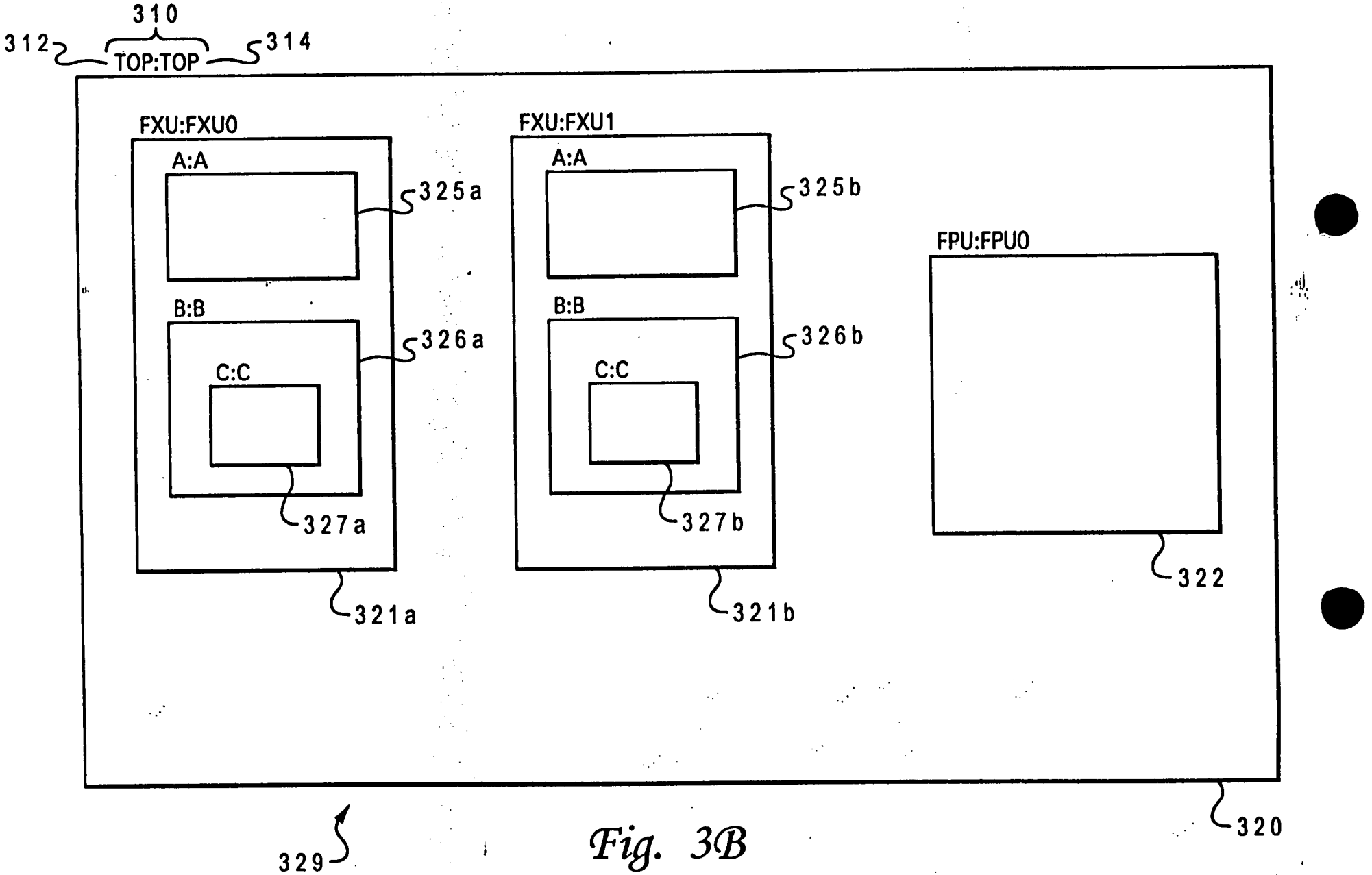

Fig. 3B

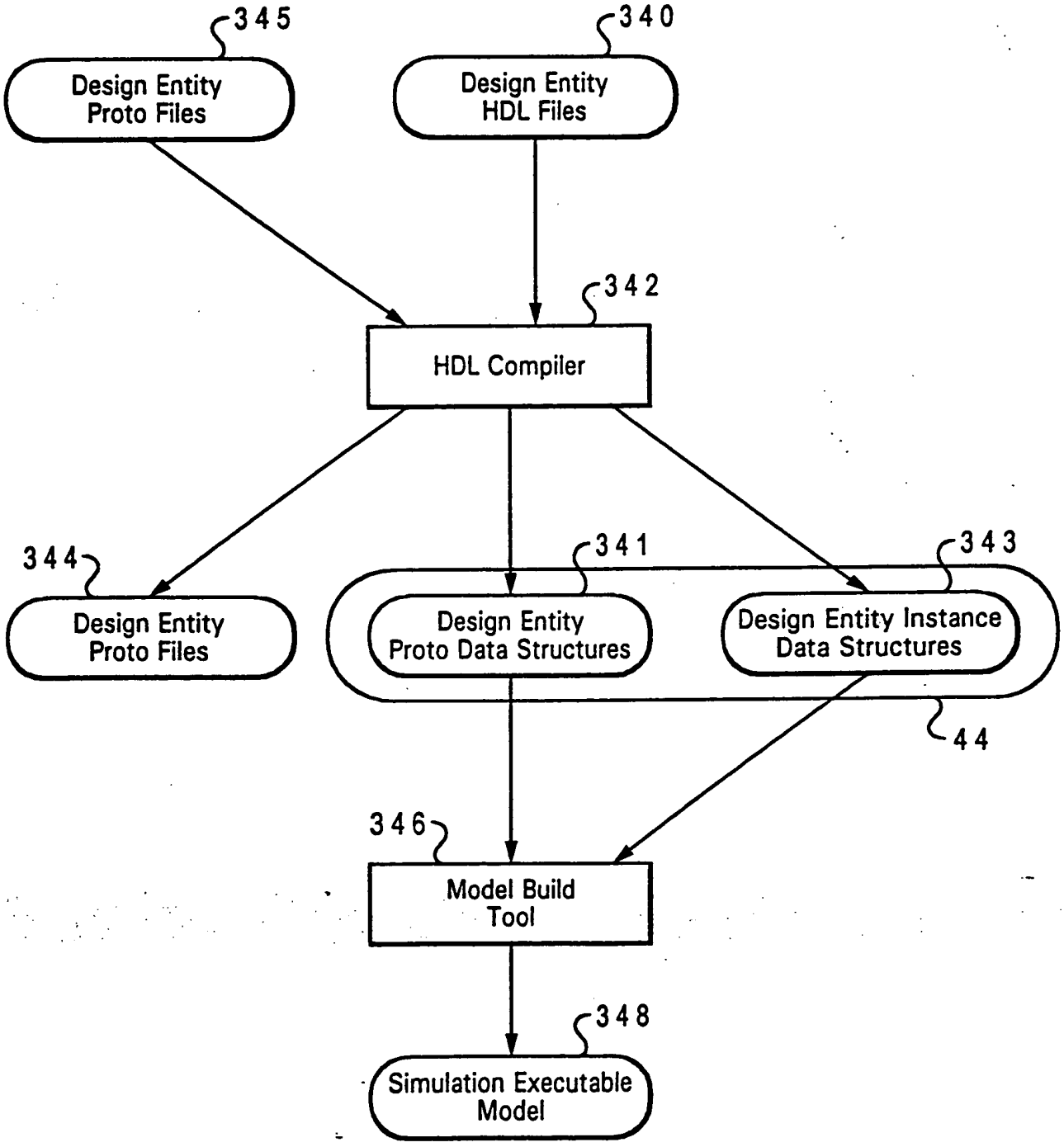
345
Design Entity
Proto Files
340
Design Entity
HDL Files
342
HDL Compiler
344
Design Entity
Proto Files
341
Design Entity
Proto Data Structures
343
Design Entity Instance
Data Structures
44
346
Model Build
Tool
348
Simulation Executable
Model

Fig. 3C

09752541 "12300

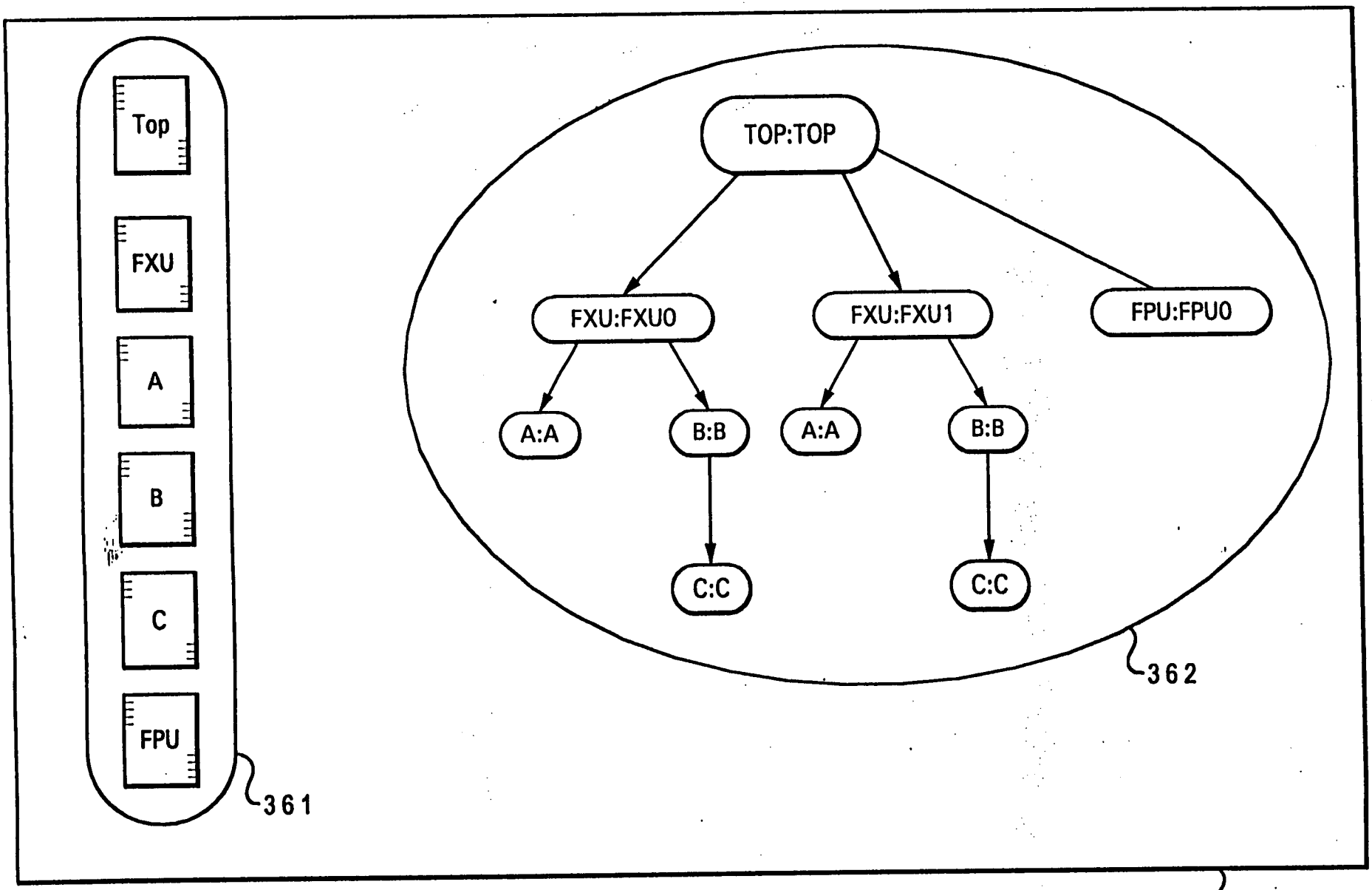

Fig. 3D

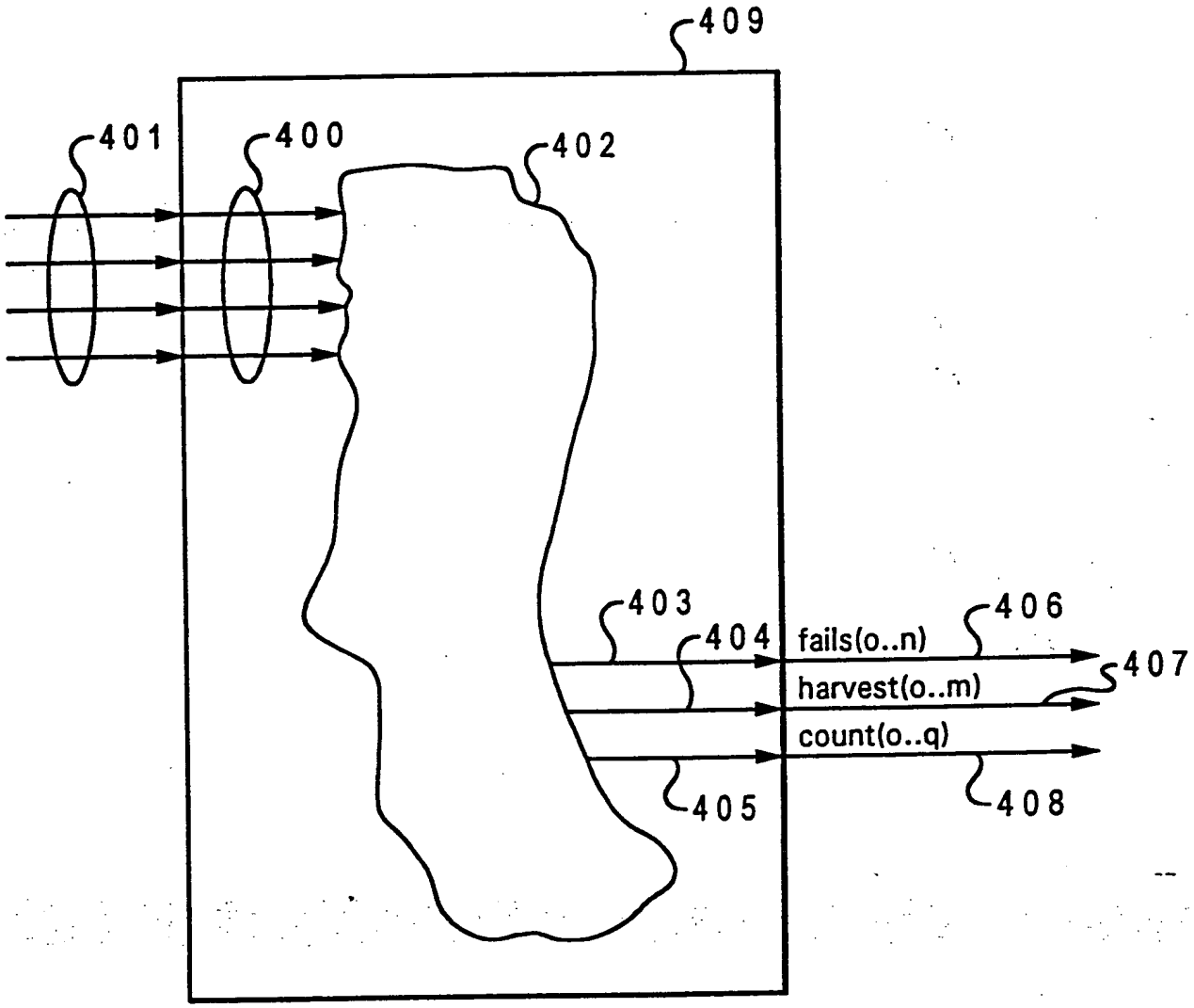
409
401
400
402
403
404
406
fails(o..n)
407
harvest(o..m)
count(o..q)
405
408

Fig. 4A

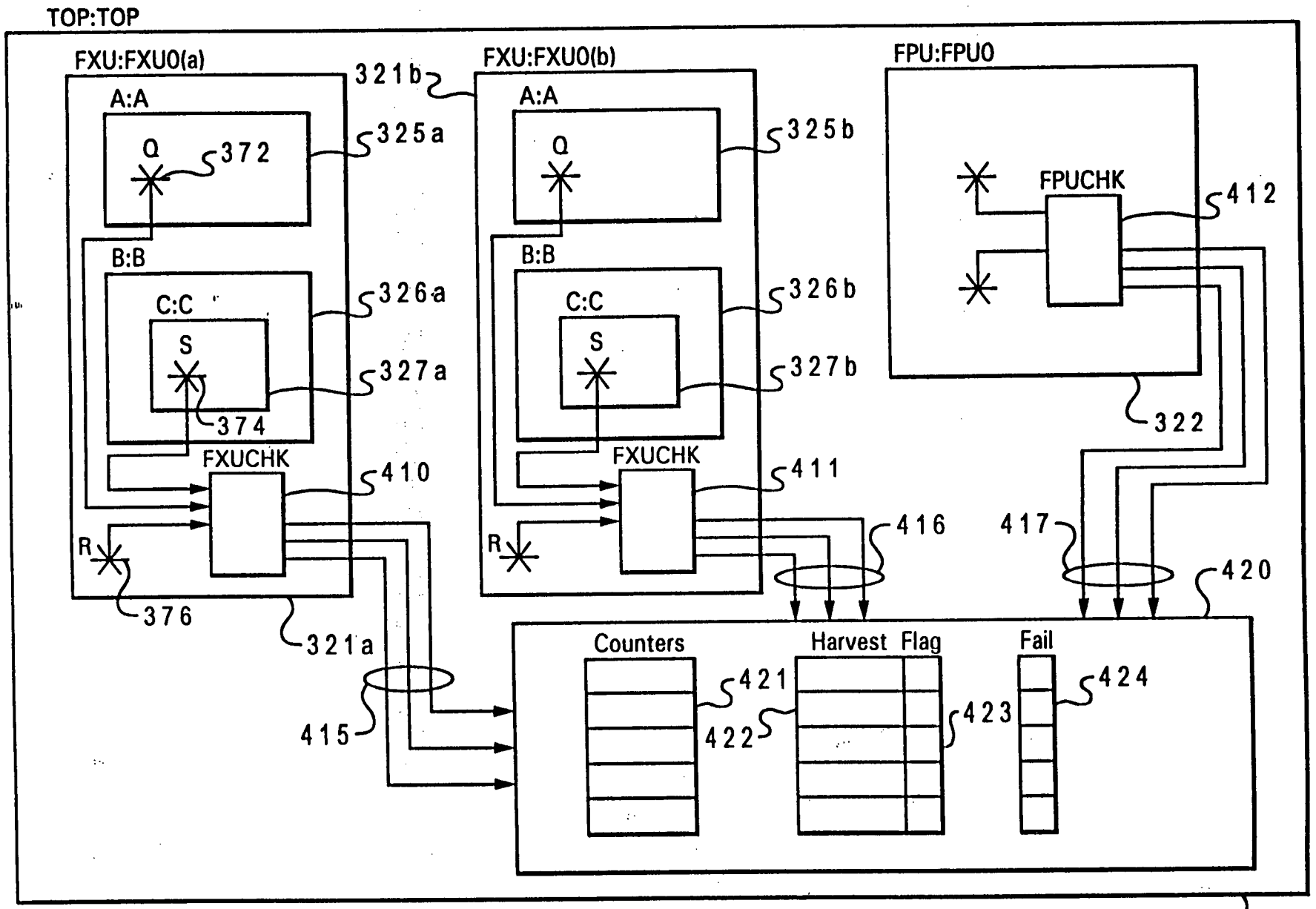
TOP:TOP
FXU:FXU0(a)
A:A
Q
372
325a
B:B
C:C
S
326a
327a
374
FXUCHK
410
R
376
321a
321b
FXU:FXU0(b)
A:A
Q
325b
B:B
C:C
S
326b
327b
FXUCHK
411
R
FPU:FPU0
FPUCHK
412
322
416
417
420
Counters
Harvest
Flag
Fail
421
422
423
424
415
329

Fig. 4B

```
ENTITY FXUCHK IS

    PORT(   S_IN        :   IN std_ulogic:
            Q_IN        :   IN std_ulogic:
            R_IN        :   IN std_ulogic:
            clock       :   IN std_ulogic:
            fails       :   OUT std_ulogic_vector(0 to 1);
            counts      :   OUT std_ulogic_vector(0 to 2);
            harvests    :   OUT std_ulogic_vector(0 to 1);
        );

--!! BEGIN
--!! Design Entity: FXU;

--!! Inputs
--!! S_IN        =>    B.C.S;
--!! Q_IN        =>    A.Q;
--!! R_IN        =>    R;
--!! CLOCK       =>    clock;
--!! End Inputs

--!! Fail Outputs;
--!! 0 : "Fail message for failure event 0";
--!! 1 : "Fail message for failure event 1";
--!! End Fail Outputs;

--!! Count Outputs;
--!! 0 : <event0> clock;
--!! 1 : <event1> clock;
--!! 2 : <event2> clock;
--!! End Count Outputs;

--!! Harvest Outputs;
--!! 0 : "Message for harvest event 0";
--!! 1 : "Message for harvest event 1";
--!! End Harvest Outputs;

--!! End;

ARCHITECTURE example of FXUCHK IS

BEGIN

    ... HDL code for entity body section ...

END;
```

450 452 453 454 455 456 457 451 458 440

Fig. 4C

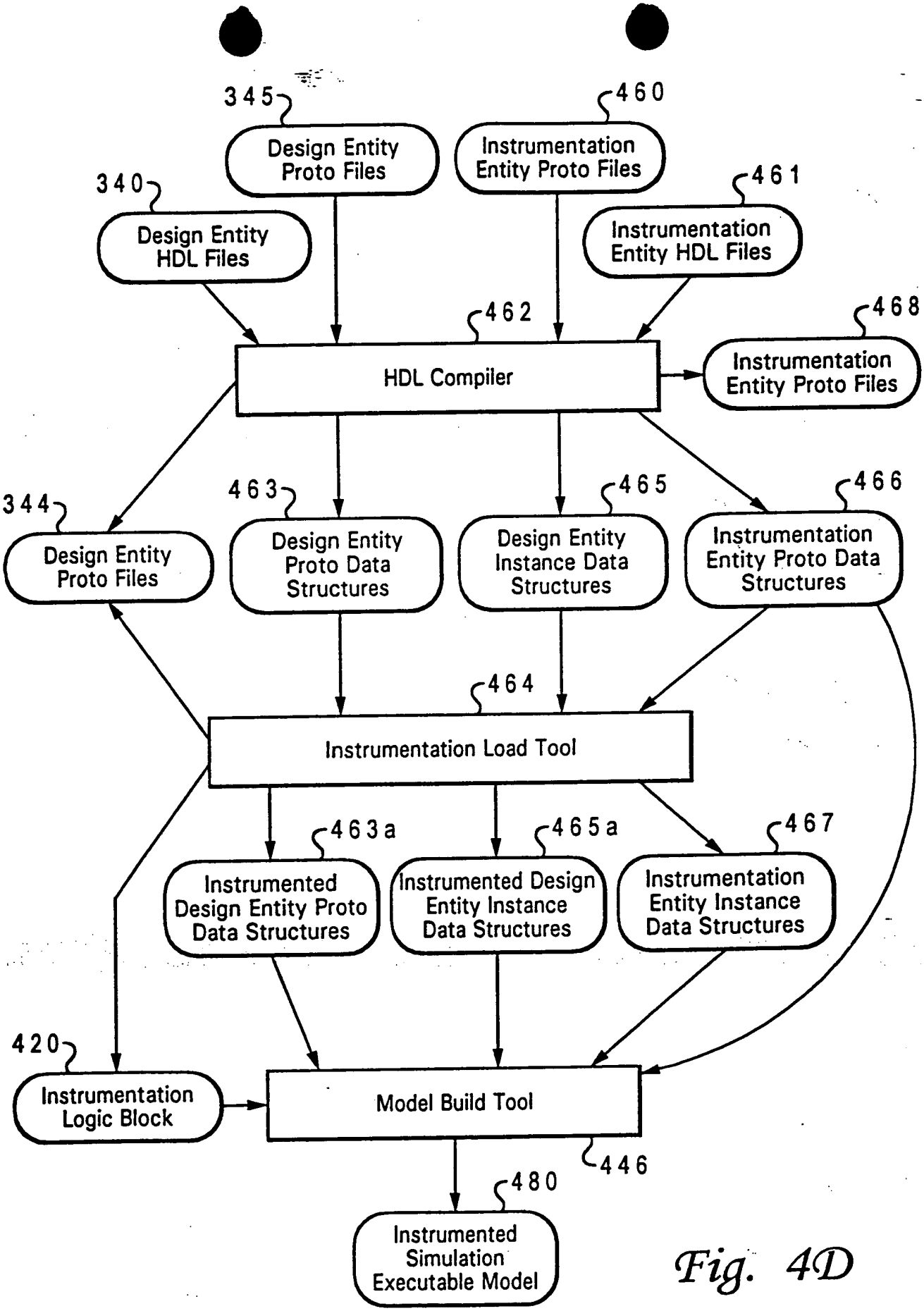
345
Design Entity Proto Files
460
Instrumentation Entity Proto Files
340
Design Entity HDL Files
461
Instrumentation Entity HDL Files
462
HDL Compiler
468
Instrumentation Entity Proto Files
344
Design Entity Proto Files
463
Design Entity Proto Data Structures
465
Design Entity Instance Data Structures
466
Instrumentation Entity Proto Data Structures
464
Instrumentation Load Tool
463a
Instrumented Design Entity Proto Data Structures
465a
Instrumented Design Entity Instance Data Structures
467
Instrumentation Entity Instance Data Structures
420
Instrumentation Logic Block
Model Build Tool
446
480
Instrumented Simulation Executable Model

Fig. 4D

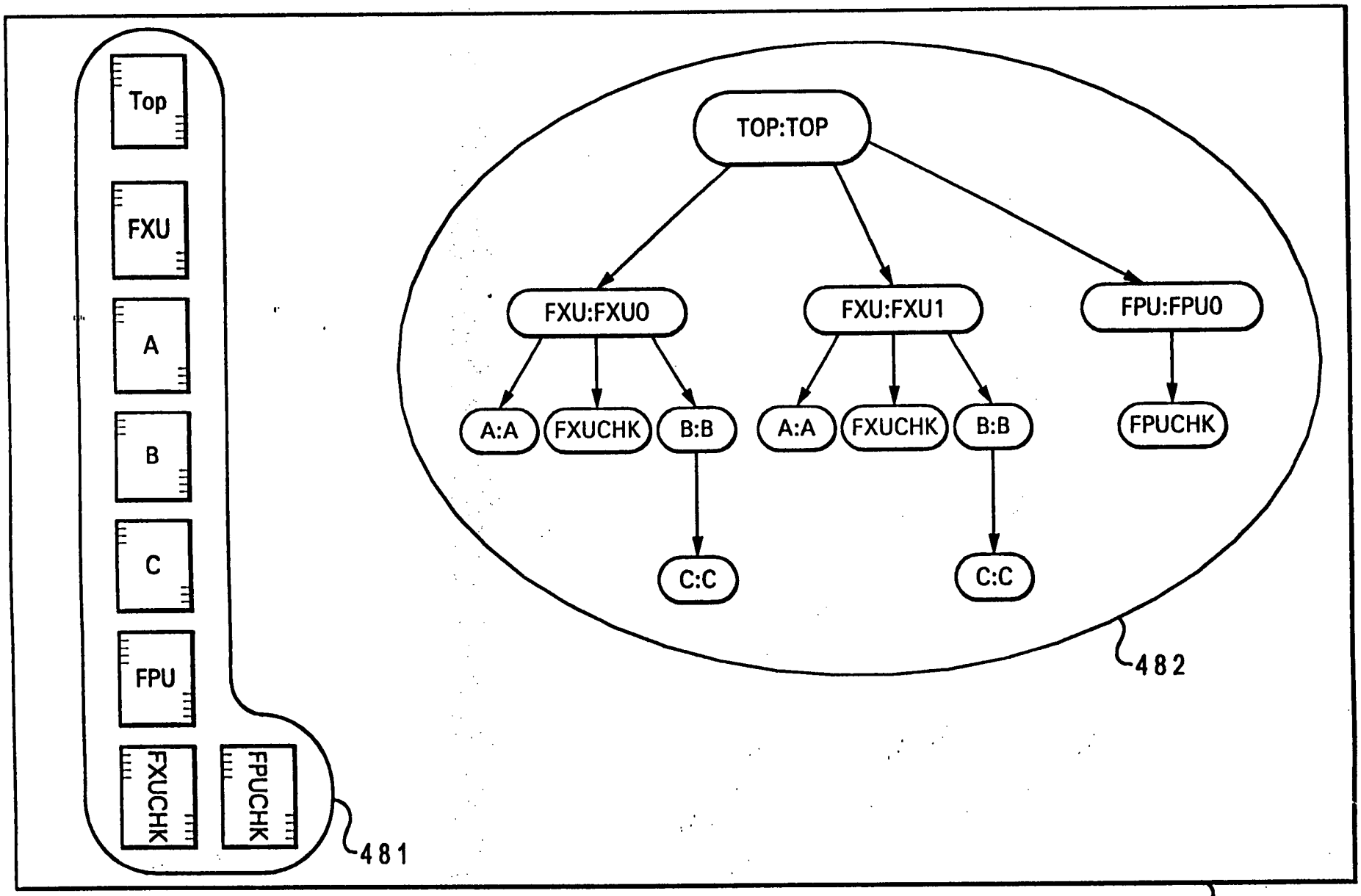
Top
FXU
A
B
C
FPU
FXUCHK
FPUCHK
481
TOP:TOP
FXU:FXU0
FXU:FXU1
FPU:FPU0
A:A
FXUCHK
B:B
A:A
FXUCHK
B:B
FPUCHK
C:C
C:C
482
44

Fig. 4E

09752251.123000

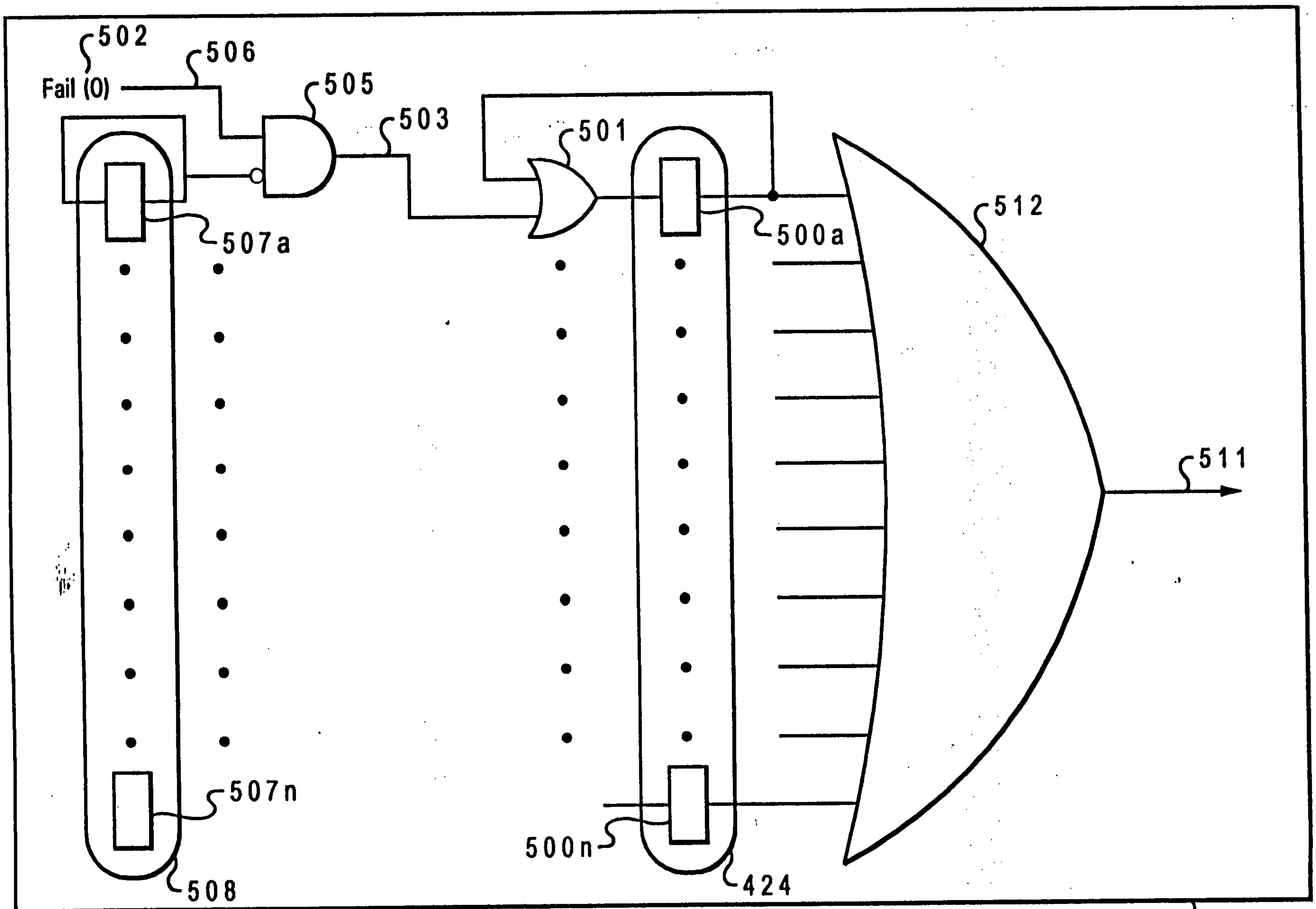

Fig. 5A

000627 "TS225760

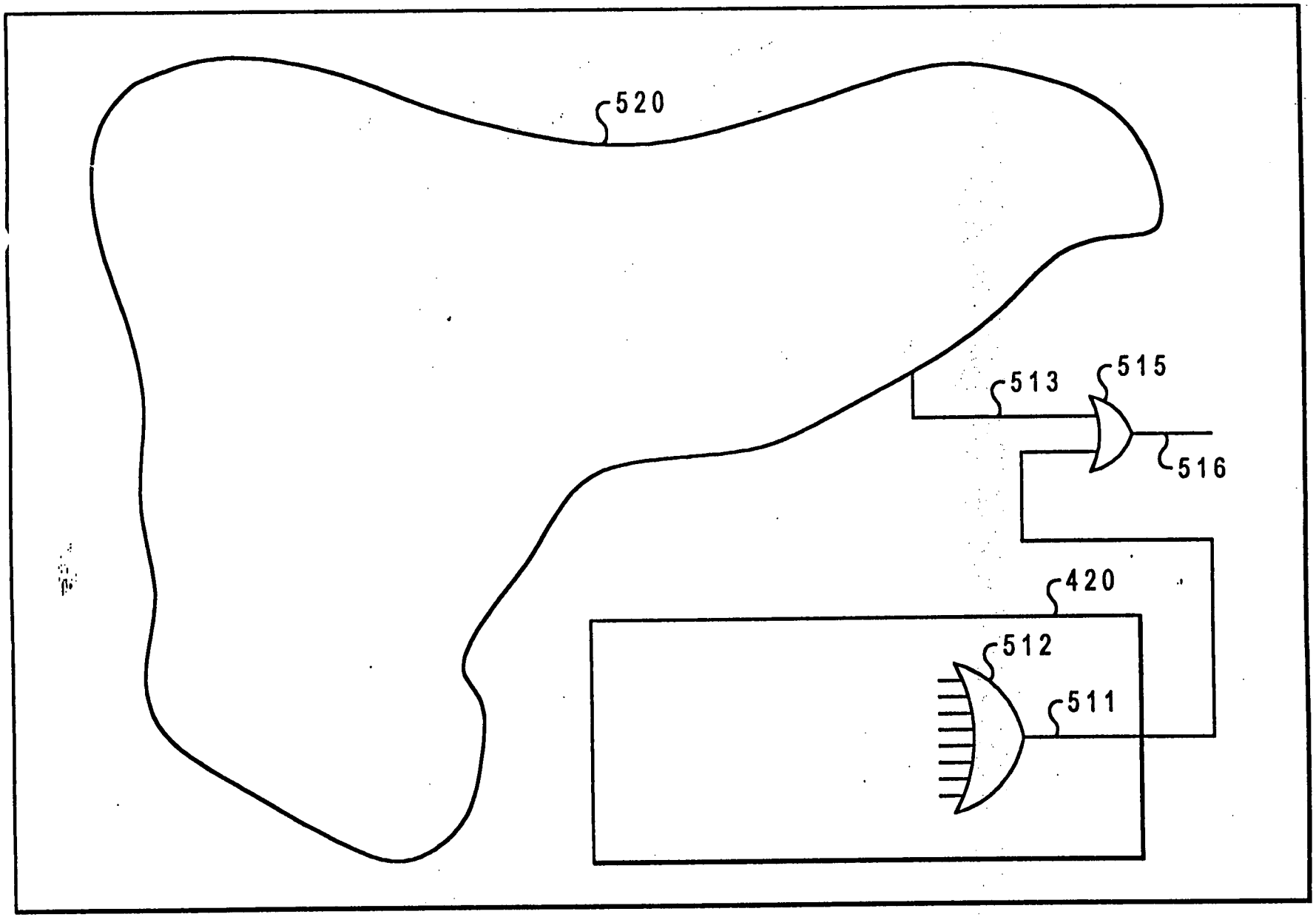

Fig. 5B

09725251.123000

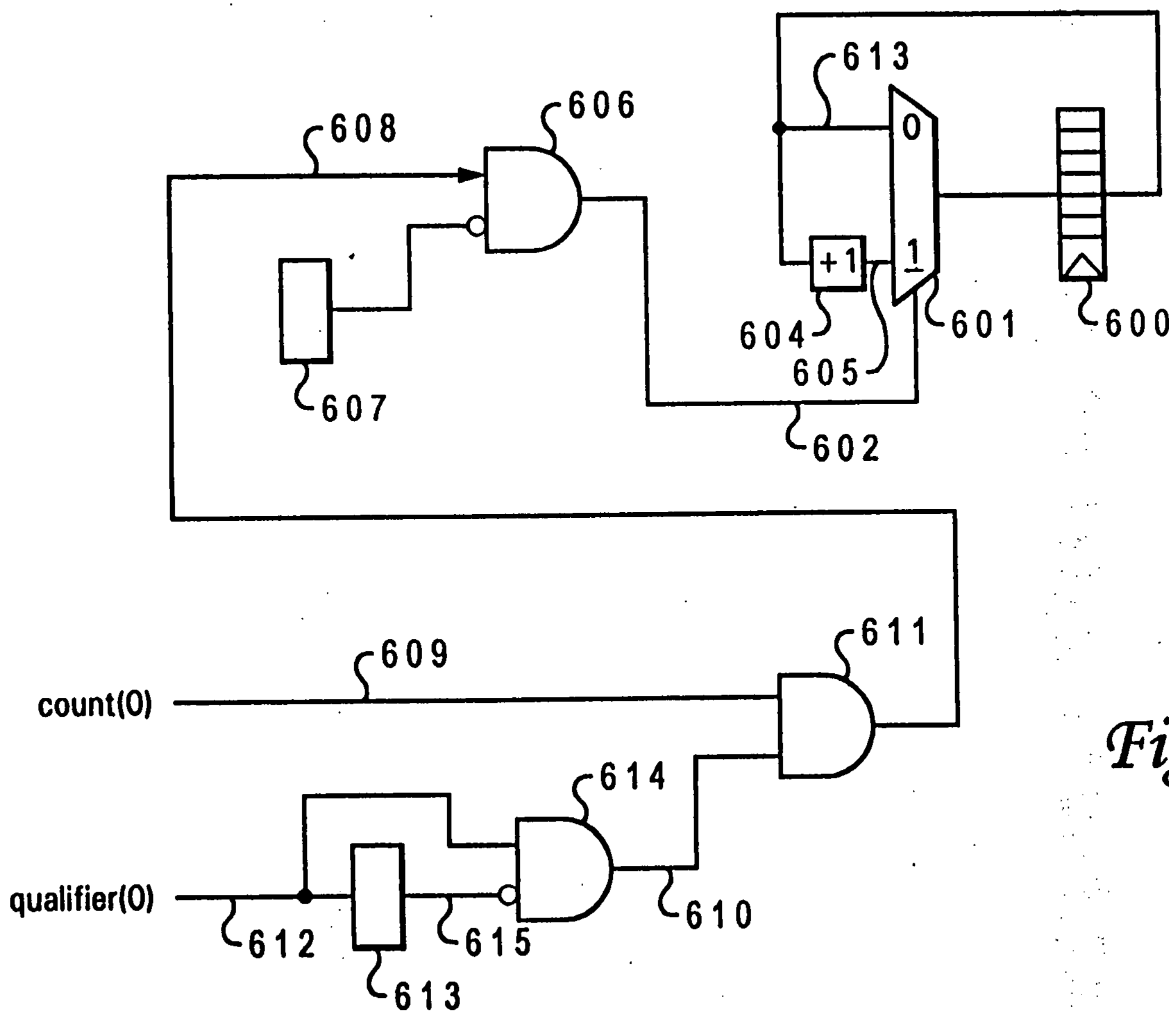

Fig. 6A

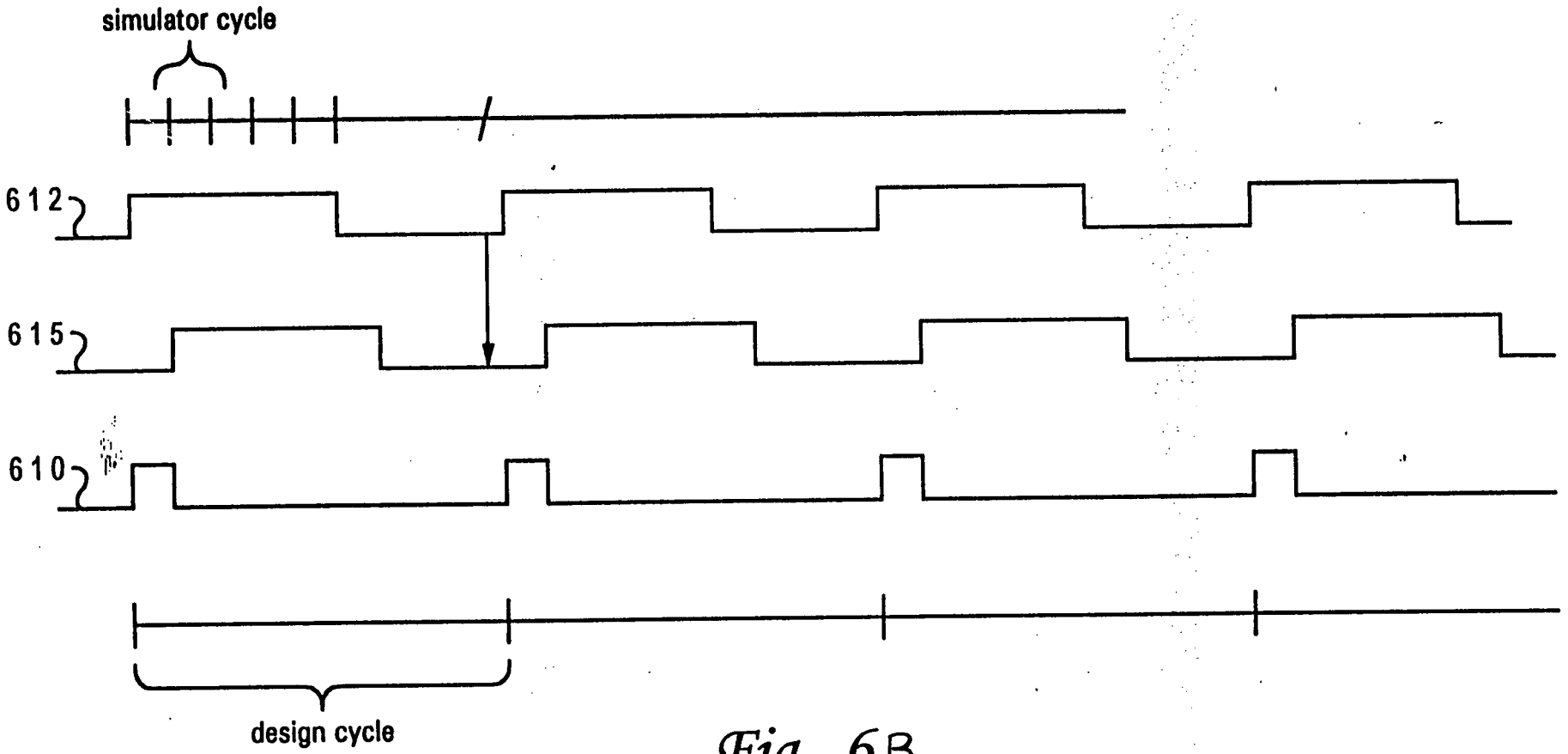

Fig. 6B

09752541 "23000

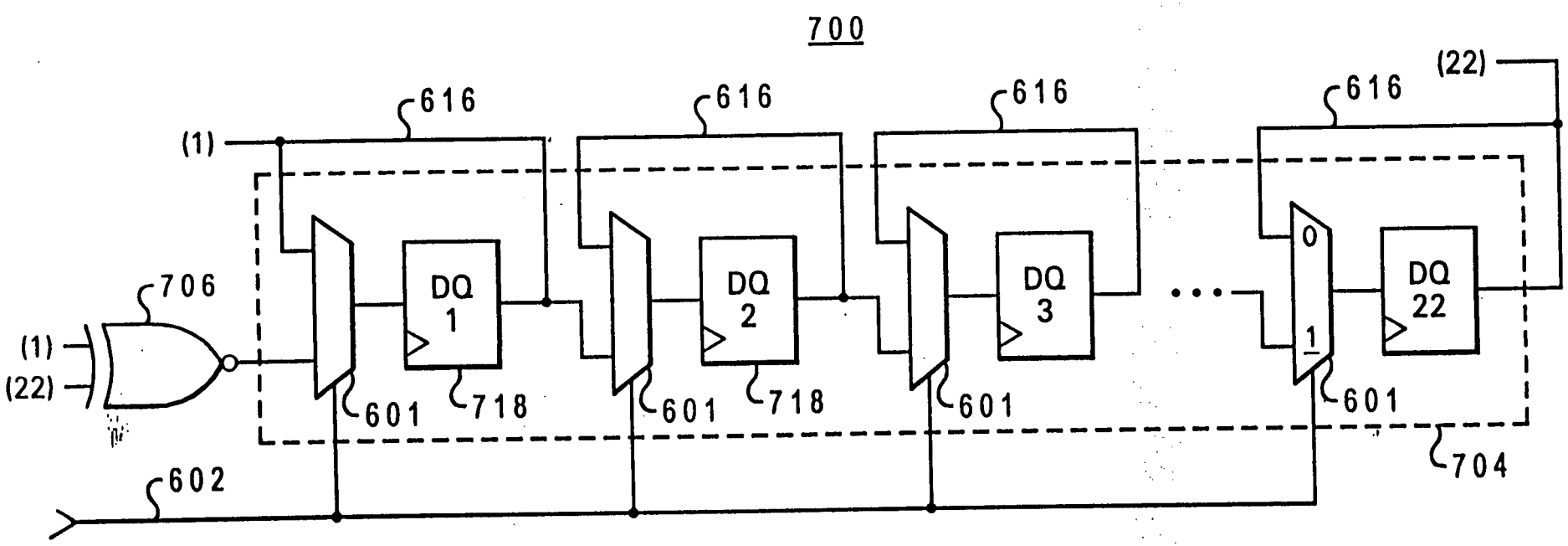

Fig. 7

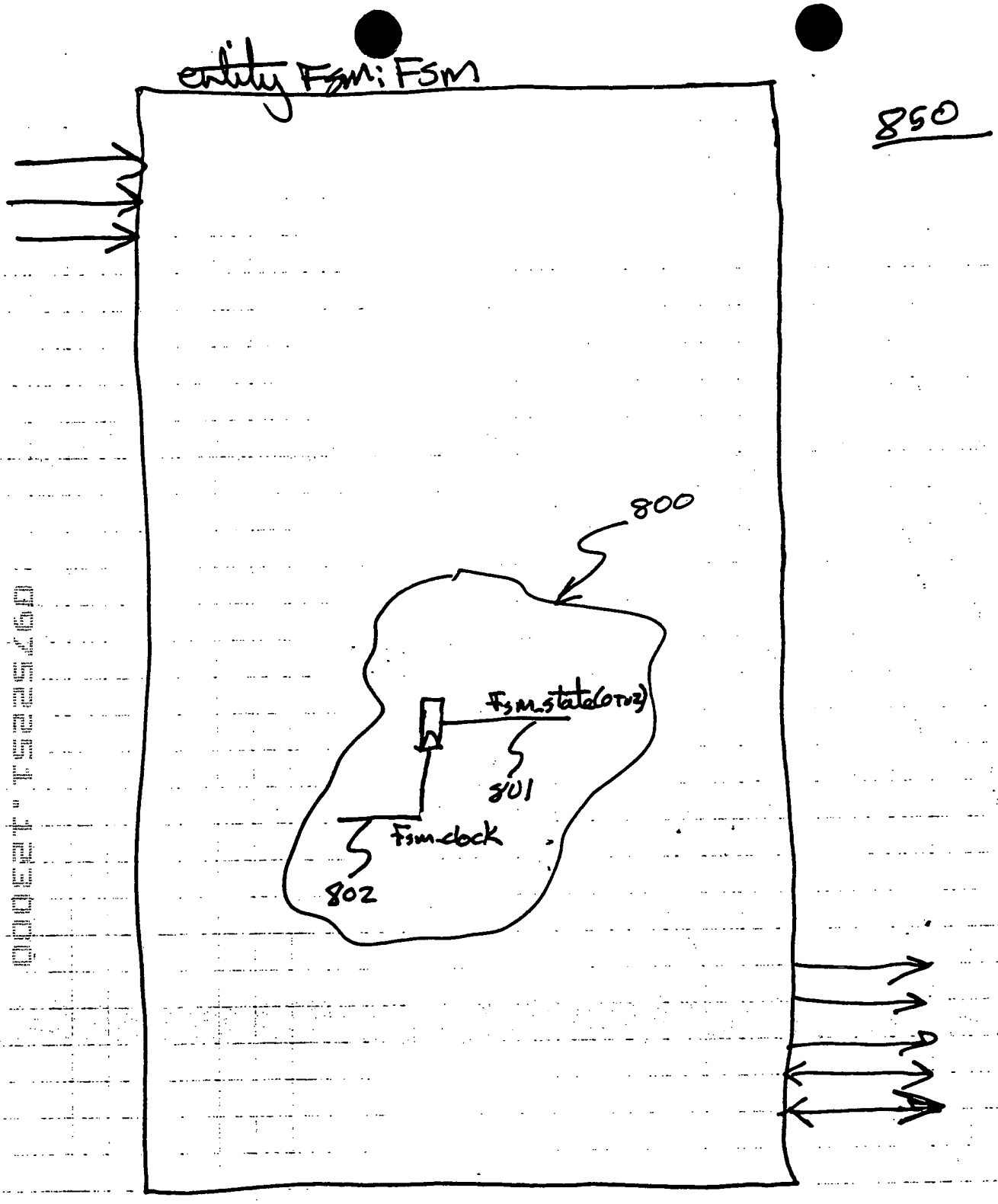

FIG. 8A
(Prior Art)

```
entity Fsm IS
  PORT(
        .... ports for entity Fsm .....
  );
ARCHITECTURE Fsm of Fsm IS
BEGIN
        .... HDL code For Fsm and rest of the entity...
        fsm_state(0 to 2) <= ... signal 801 ....
853 {   --!! Embedded FSM : exampleFsm;
859 {   --!! clock         : (fsm_clock);
854 {   --!! state_vector  : (fsm_state(0 to 2));
855 {   --!! states        : (s0,s1,s2,s3,s4);
856 {   --!! state_encoding: ('000','001','010','011','100');
857 {   --!! arcs          : (s0=>s0, s0=>s1, s0=>s2,
        --!!                 s1=>s2, s1=>s3, s2=>s2,
        --!!                 s2=>s3, s3=>s4, s4=>s0);
858 {   --!! end Fsm;
END;
```

852

856

FIG. 8B

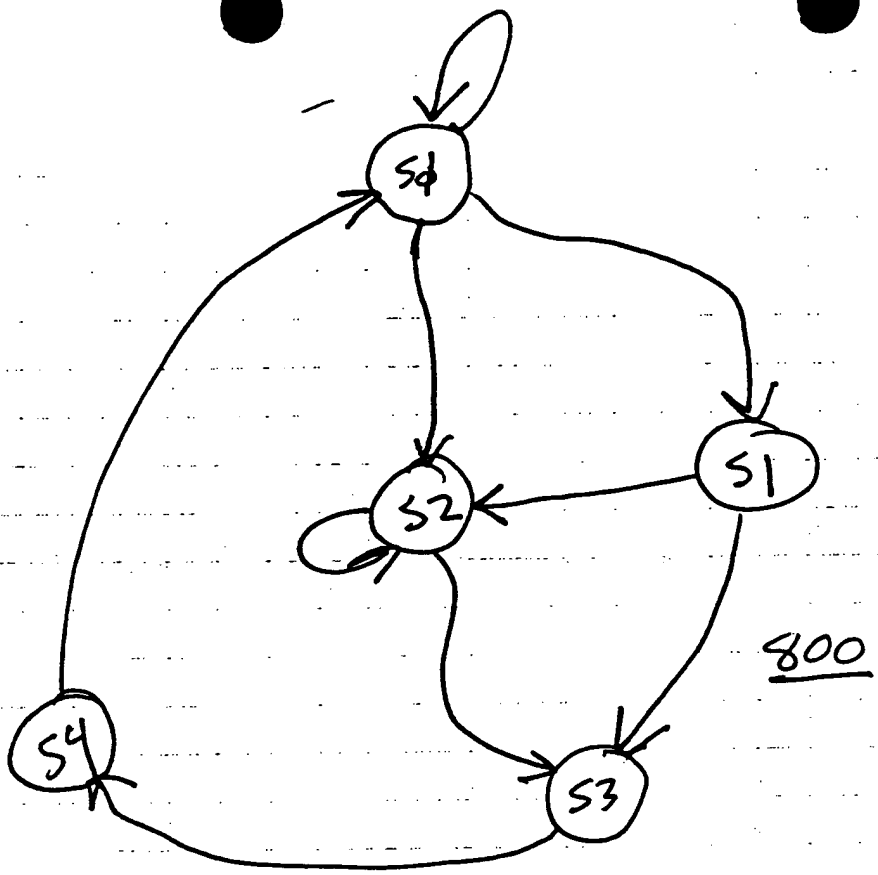

FIG. 8

(Prior Art)

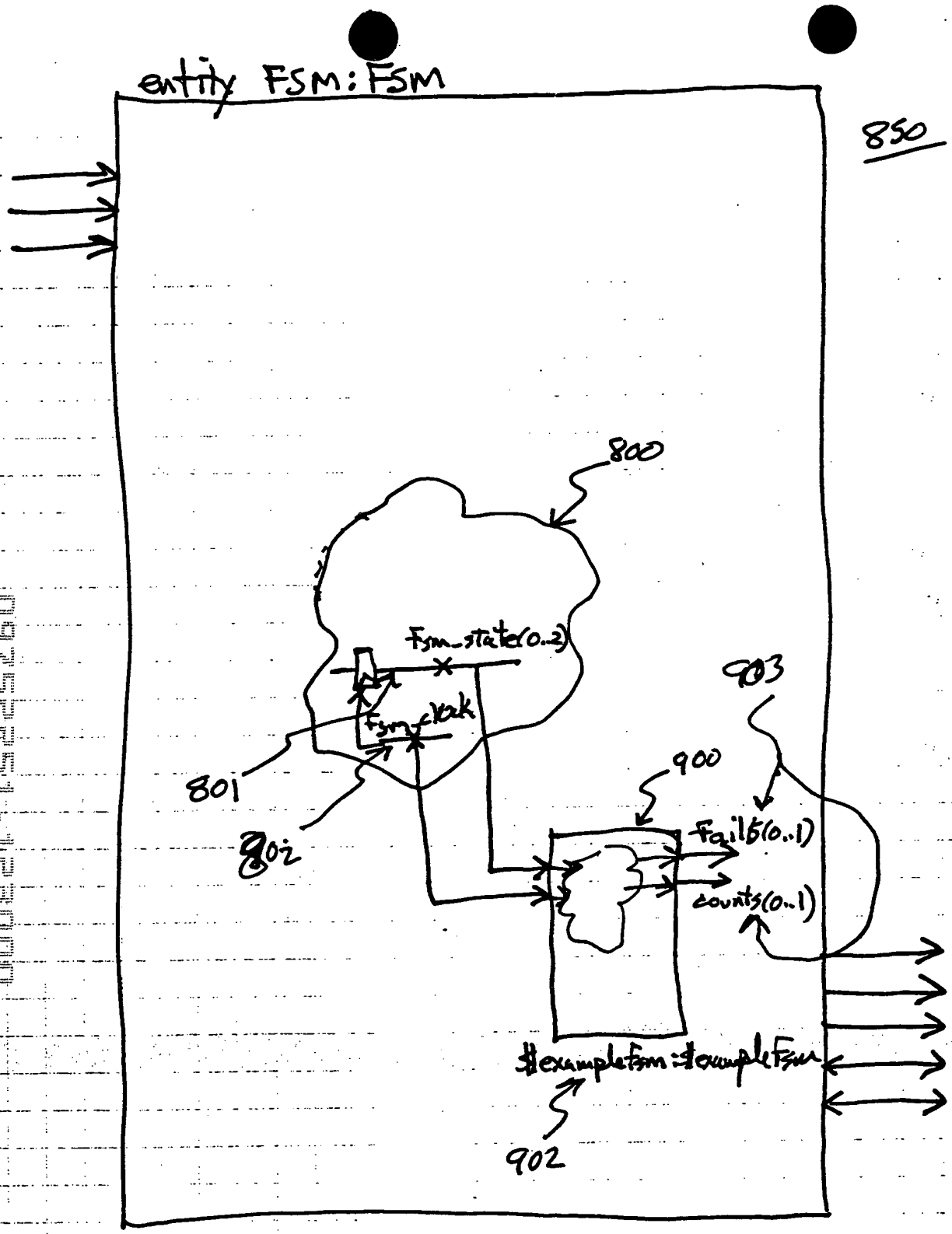
entity FSM: FSM
850
800
Fsm_state(0..3)
Fsm_clock
801
802
903
900
Fail5(0..1)
counts(0..1)
#examplefsm: #exampleFsm
902

FIG. 9

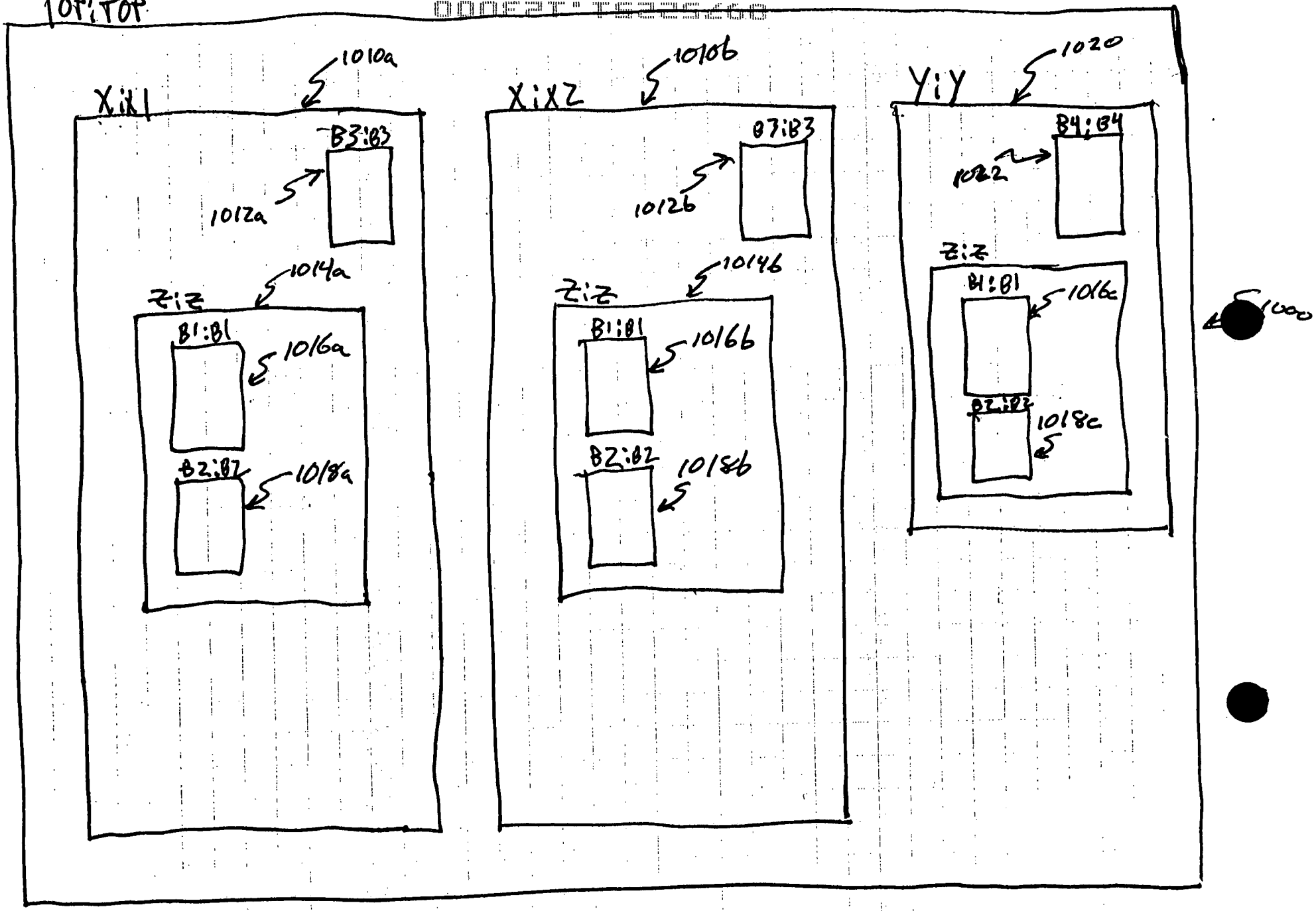
TOP:TOP
1010a
X:X1
B3:B3
1012a
Z:Z
1014a
B1:B1
1016a
B2:B2
1018a
1010b
X:X2
B7:B3
1012b
Z:Z
1014b
B1:B1
1016b
B2:B2
1018b
1020
Y:Y
B4:B4
1022
Z:Z
B1:B1
1016c
B2:B2
1018c
1000

FIG. 10A

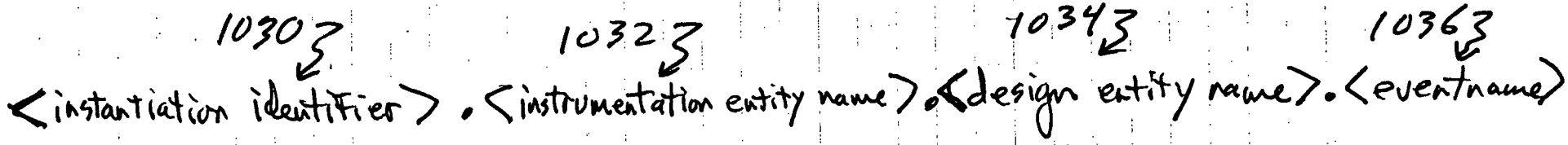

FIG 10B

1030	1032	1034	1036	
X1	B3	X	COUNT1	1040
X1.Z	B1	Z	COUNT1	1041
X1.Z	B2	Z	COUNT1	1042
X2	B3	X	COUNT1	1043
X2.Z	B1	Z	COUNT1	1044
X2.Z	B2	Z	COUNT1	1045
Y	B4	Y	COUNT1	1046
Y.Z	B1	Z	COUNT1	1047
Y.Z	B2	Z	COUNT1	1048

FIG 10C

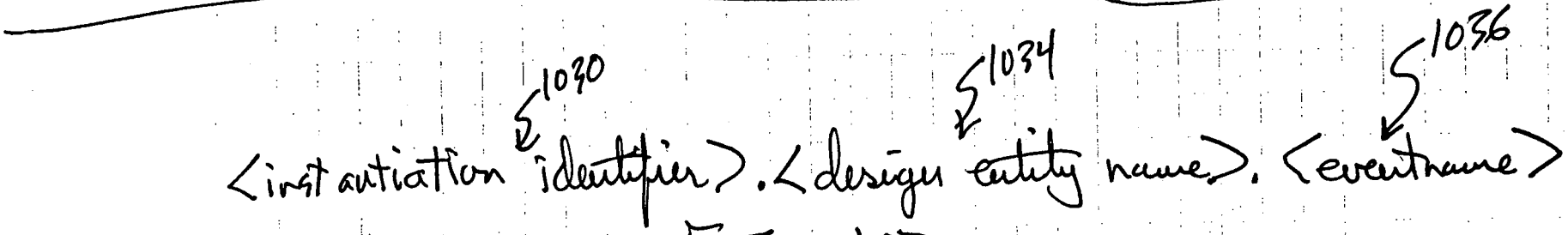

FIG. 10D

DOCKET TS225260

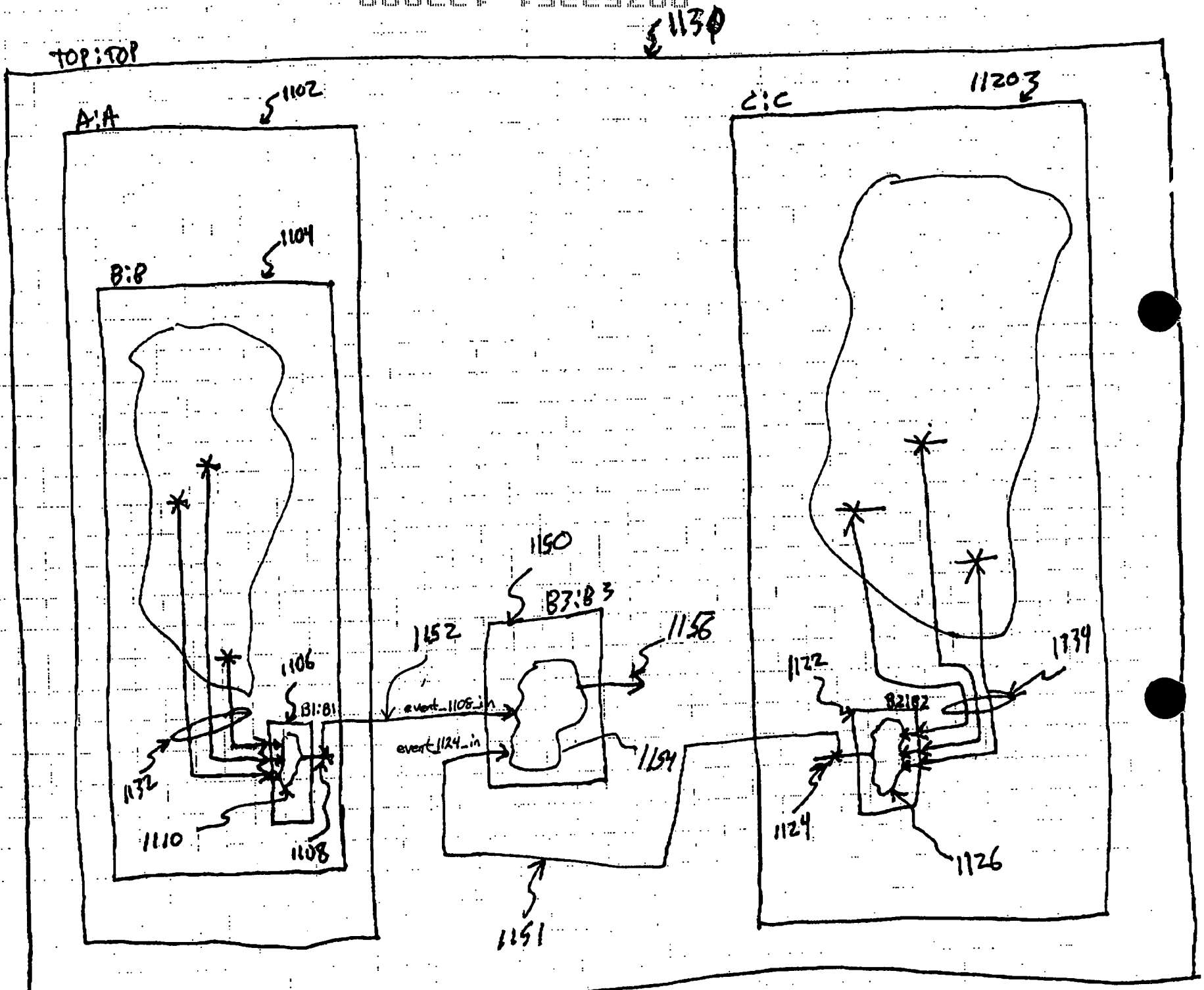

FIG. 11A

DEC 11 '00 12:13 FR 512#838#5882 512 838 5882 TO 93436002 P.02/03

000621 "T5225760

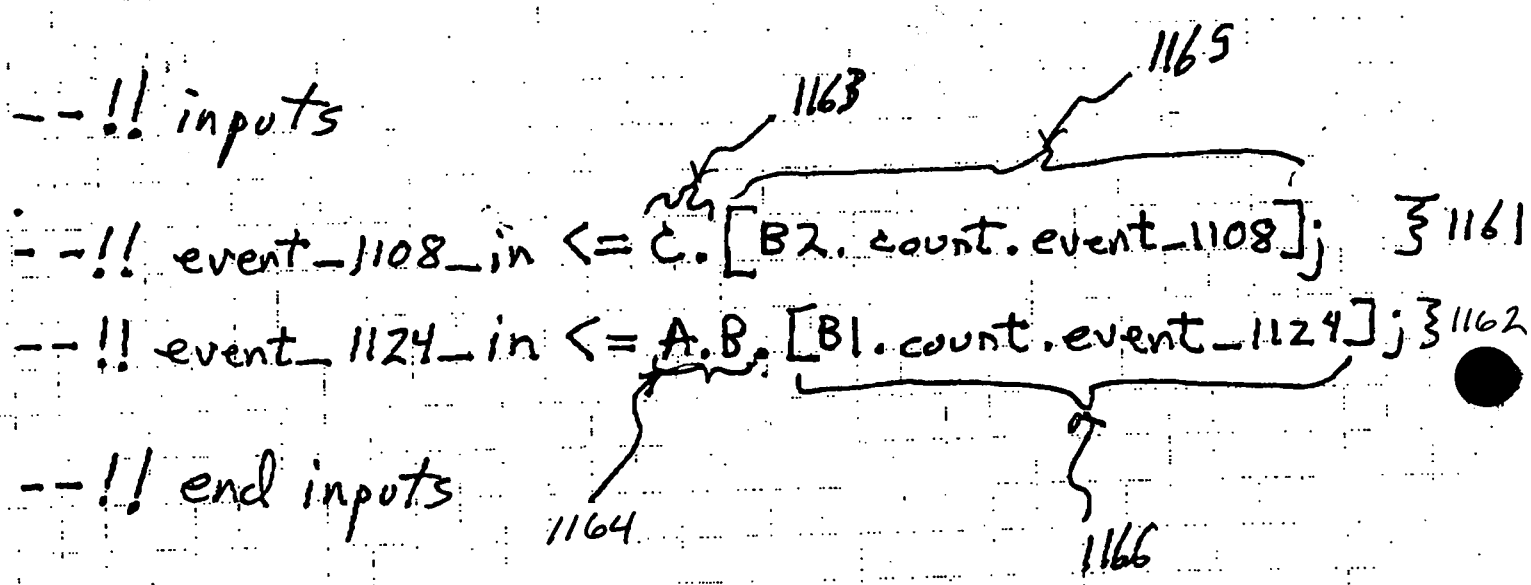

FIG. 11B

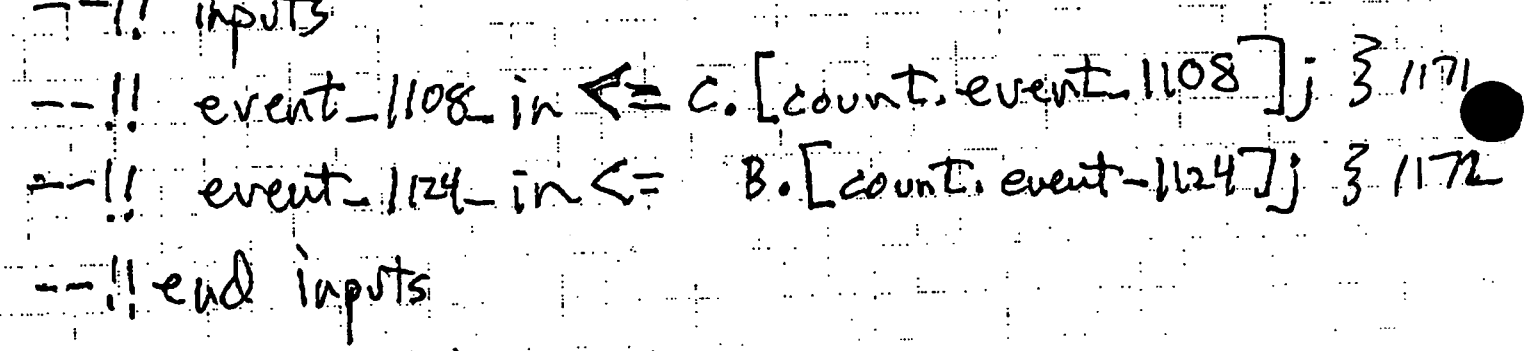

FIG. 11C

DEC 11 '00 12:14 FR 512#838#5882 512 838 5882 TO 93436002 P.03/03
** TOTAL PAGE.03 **

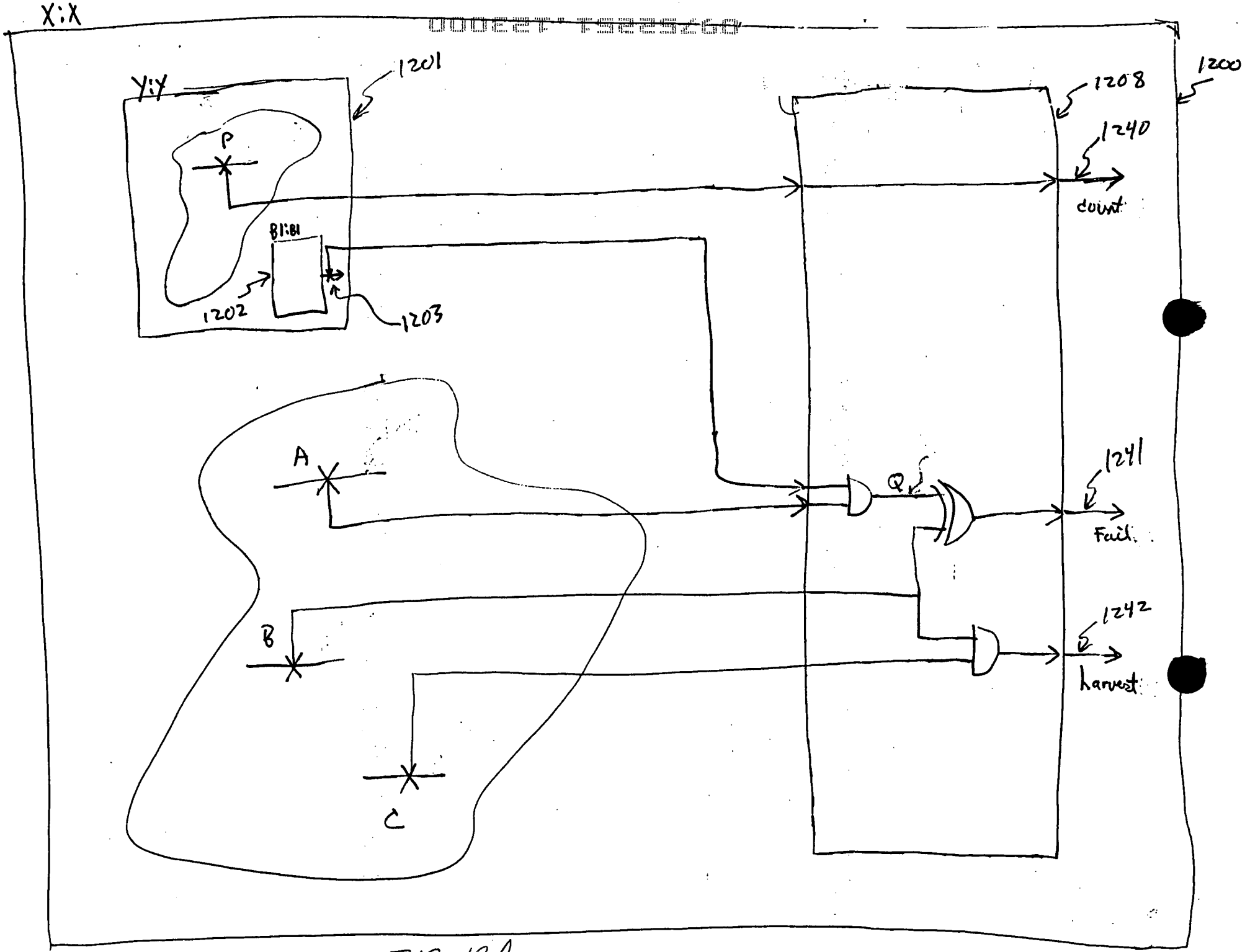
X:X
Y:Y
1201
1200
1208
1240
count
P
B1:B1
1202
1203
A
B
C
Q
1241
Fail
1242
harvest

FIG. 12A

```
Entity X IS
    PORT (
        ...
    );
ARCHITECTURE example OF X IS
BEGIN
    ...
    ...HDL CODE FOR X.....
    ...
    Y:Y                                  } 1221
    PORT MAP(;                           }
        );                               }
    A <= ....                            } 1222
    B <= ....                            }
    C <= ....                            }
    --!! [count, countname0, clock] <= Y.P;        } 1230
    --!! Q <= Y.[B1.count.count1] AND A;           } 1232
    --!! [fail, Failname0, "fail msg"] <= Q XOR B; } 1234
    --!! [harvest, harvestname0, "harvest msg"] <= B AND C; } 1236   } 1223
    ...
END
```

FIG. 12B